Growing Multiple Compound Semiconductors on a Single Substrate

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Introduction

In Dr. Kapadia's Lab, I am working along with my PhD mentor to grow multiple compound semiconductors on a single substrate of materials other than Silicon. Currently, only similar semiconductors are grown together due to varying growth conditions for each semiconductor. The researchers want to grow different semiconductors on one substrate in order to improve the functionality of the semiconductor chips that potentially could be used in electronic devices. My work in the research was to simulate the heat transfer along the heat barrier of the samples which would provide the required heat for the growth while not damaging other elements.

Objectives & Impact of Professor's Research

The objective of the Professor's Research is to improve the functionality and increase efficiency of the semiconductor processor present in current electronic devices. The current method of growing compound semiconductors involving growing and placing individual atoms or molecules of the semiconductor upon the substrate and heating them up separate from other components of the processor. The devised method of growing semiconductors in the research requires to arrange the compound semiconductors in the desired shape as required for the functionality of the processor and then heating up all the components together. The pre-arrangement of the compound semiconductor upon the substrate should be beneficial since the shape of the semiconductors are predetermined and will not be misshaped as it is possible with the current method of growing semiconductors.

Methods & Data

Initially, I had to find the heat required for the given temperature difference across a silicon dioxide slab of 100 nm. I solved the problem by hand using Fourier's Law equation. Later, I worked on COMSOL Multiphysics - a computer application which allowed simulations for various scientific purposes – to simulate the heat transfer through the heat barrier and verify the hand calculated results. The hand calculation and simulation results matched up.

Figure 1

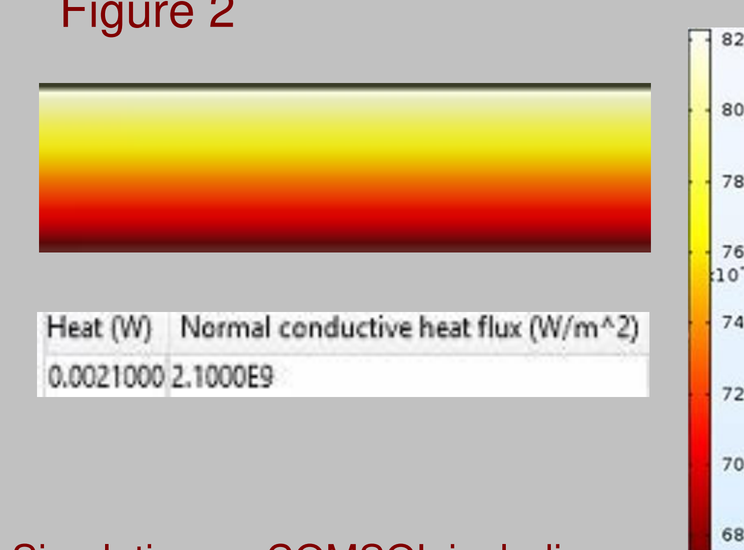
$$Q = \frac{k}{s} \times A \times dT$$

$$Q = \frac{1.4\ W/m°C}{1\times10^{-9}\ m} \times (10^{-6}m \times 10^{-6}m) \times (550°C\ - 400°C)$$

$$Q\ = 0.0021\ W$$

Calculations using Fourier's Law to for heat required upon surface of given dimensions

Figure 2



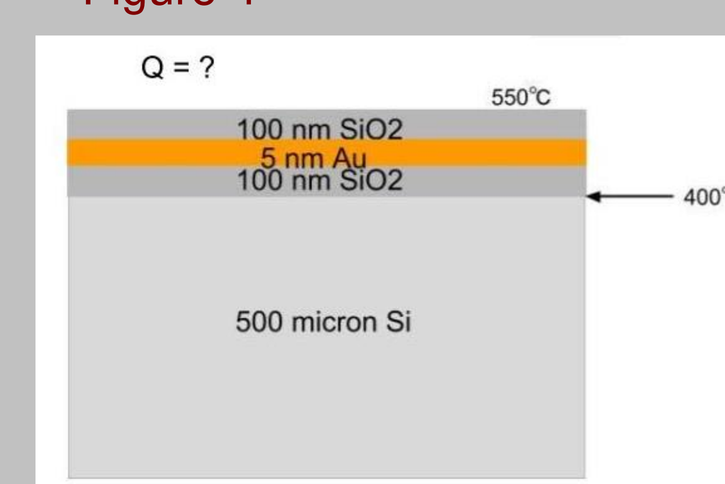
Simulation on COMSOL including temperature map and numerical values.

The purpose of simulating was to find out what was the required heat flux to provide the required growth temperature on the Silicon Dioxide heating surface, (550 °C) and retain a lower temperature (400 °C) across the heat barrier between the Silicon Dioxide and Silicon joint that would not a damage the other parts of the processor.

Figure 3

The first configuration of the heat barrier: a layer of Silicon Dioxide over a slab of Silicon.

Figure 4

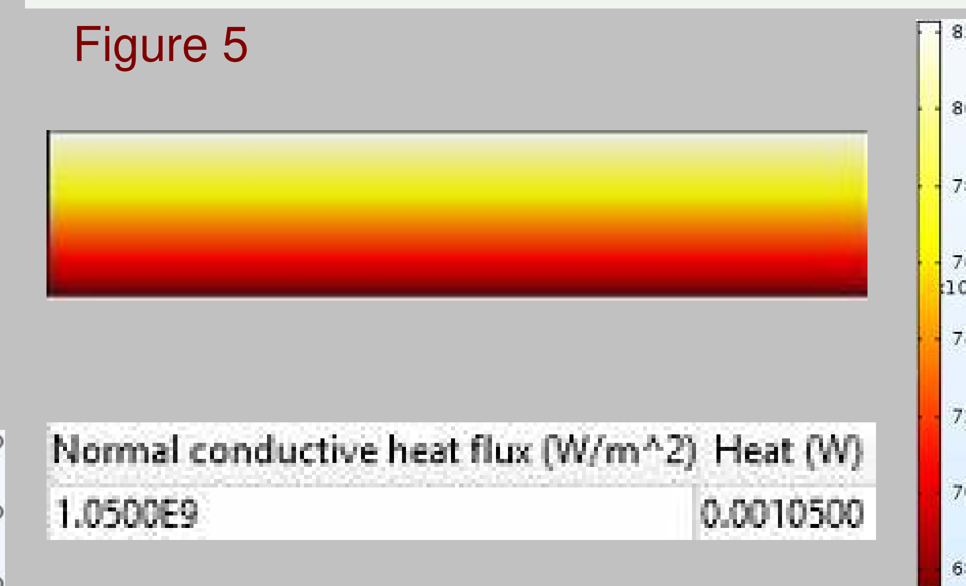


The second configuration of the heat barrier including a Gold reflector in between two Silicon Dioxide layers.

Results

The results for the First configuration of the heat barrier, with Silicon Dioxide upon Silicon shows that the thermal annealing upon the heating surface required a heat flux of $1.050 \times 10^{9}\ W/m°C$

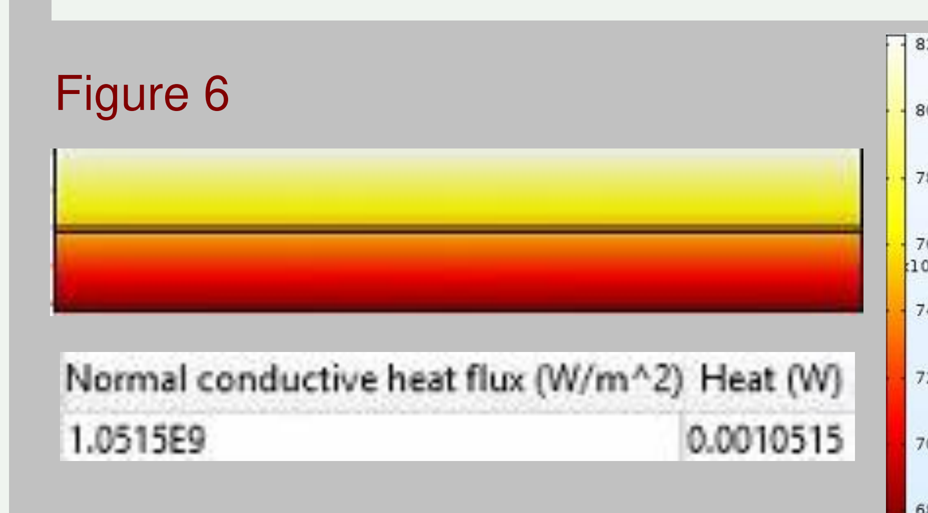
Figure 5



Temperature map of the Silicon Dioxide heat barrier with derived numerical values for heat and heat flux

The results for the second configuration, with the Gold reflector between two Silicon Dioxide layers shows that the thermal annealing required a heat flux of $1.051 \times 10^{9}\ W/m°C$.

Figure 6



Temperature map of the Silicon Dioxide, Gold reflector heat barrier with derived numerical values for heat and heat flux

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